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TOWARD HIGH PERFORMANCE N/P GAAS SOLAR CELLS GROWN ON LOW DISLOCATION DENSITY P-TYPE SIGE SUBSTRATES

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ABSTRACT

GaAs solar cells grown on SiGe/Si virtual substrates in the n/p configuration are of interest to develop III-V/Si cell technologies with high radiation-tolerance and to demonstrate the general applicability of SiGe/Si substrates for transfer of standard multi-junction configurations. This paper reports the first study of minority carrier electron lifetimes in p-type GaAs base materials grown on low dislocation density ($1x10^6$ cm^{-2}) SiGe/Si substrates and the first study of n/p III-V cells grown on SiGe as a function of threading dislocation density. Minority carrier diffusion lengths of ~ 4 μm, well in excess of a typical n/p cell base thickness, are demonstrated and correlations between diffusion length and dislocation density are made. Preliminary cell results match theoretical predictions, and n/p GaAs cell efficiencies on Si in excess of 15% have been achieved. In parallel developments for p/n cells, GaAs cell areas on SiGe have been increased from 0.36 cm^2 to 4 cm^2 with no decrease in cell performance. This indicates that thermal stress induced microcracks are not limiting cell performance on SiGe/Si substrates at this stage of development. The cumulative impact of these results indicate the growing promise of SiGe virtual substrates for achieving high performance III-V solar cells grown on Si substrates utilizing SiGe buffer layers.

1. INTRODUCTION

III-V solar cells grown on Si substrates are receiving renewed and intense interest primarily due to recent breakthroughs in the ability to achieve low dislocation density "virtual" substrates on Si that provide a suitable template for high-quality III-V overgrowth. We have shown in recent work, that SiGe step-graded, relaxed buffers reproducibly yield threading dislocation densities of $1x10^6$ cm^{-2} or below in the relaxed Ge cap layers, which when combined with monolayer-scale control of GaAs nucleation on these "virtual Ge" substrates to eliminate anti-phase domains, translate into the highest reported minority carrier (hole) lifetimes for n-GaAs on Si and highest reported V_{oc} values for p/n GaAs cells on Si to date.[1,2,3] However, while p/n cell development is ongoing, it is of great interest to extend the use of SiGe virtual substrates to n/p configuration III-V cells, which are considered to be superior in radiation-tolerance, have the potential advantage of a convenient Ge bottom cell in a multi-junction structure, and are compatible with current industry standard cell technologies. Hence, in this paper, we report the first study of p-type GaAs and n/p GaAs solar cells grown on low dislocation density, compositionally graded, relaxed p-type SiGe buffers on Si. Long diffusion lengths in the p-GaAs are confirmed and promising cell results that match theoretical expectations are achieved. In addition, we report the continued development of our p/n GaAs/Si cells, with the demonstration of a 100x increase in cell area compared to our earlier results, up to 4 cm^2, with negligible loss of cell performance.

2. EXPERIMENTAL

Step-graded SiGe buffers were grown by chemical vapor deposition on (001) Si wafers with a 6° off-cut toward the [110] direction. All SiGe growths were done on 6-inch and 8-inch diameter Si wafers. The SiGe grading procedure has been reported in earlier publications.[4] The residual threading dislocation density (TDD) in the fully relaxed Ge cap layer, which forms the virtual Ge substrate, was determined to be ~$1x10^6$ cm^{-2} for both n and p-type substrates as confirmed by plan-view transmission electron microscopy and etch pit density (EPD) measurements.[4] For all growths reported in this paper, GaAs nucleation was performed on Ge/SiGe/Si using solid source molecular beam epitaxy (MBE) as described elsewhere [1,5], followed by low pressure metalorganic chemical vapor deposition (MOCVD) for growth of n/p and p/n single junction GaAs cells and InGaP/GaAs/InGaP double heterostructures (DH) used for time-resolved photoluminescence (TRPL) lifetime measurements. DH structures were grown with GaAs layer thicknesses of 0.5, 1 and 1.5 μm with nominal doping values that match those used for the base region of the cell structure to be described below. All solar cell and DH structures were grown at 620°C. For the cells, $In_{0.5}Ga_{0.5}P$ window layers and back surface fields were used. The p/n cell had an emitter thickness of 0.5 μm and a base thickness of 2.0 μm. The n/p cell utilized a 0.05 μm emitter thickness and a 2.5

μm base thickness. In both the n/p and p/n cells, the base and emitter doping values were ~2×10^{17} cm^{-3} and ~2×10^{18} cm^{-3}, respectively. No attempts were made to optimize cell designs with respect to substrate dislocation density at this time. The cells were electrically isolated by mesa-etching and the contact layers were removed with selective-etching just prior to the antireflection coating (ARC) deposition. Front contact was made to a highly doped GaAs contact layer; Cr/Au was used for contact to p-type GaAs and Ni/Ge/Au was used for contact to n-type GaAs; Al was used for both p-type and n-type back contacts to silicon. The anti-reflection coating deposited was 75Å MgF_2 / 480Å ZnS / 990Å MgF_2. The cells range in size from 0.044 cm^2 to 4 cm^2 with metal coverage from 10% to 7%, respectively. Solar cell structures were evaluated by dark current density versus voltage (J-V), light J-V under AM0 and AM1.5 illumination, and spectral response measurements.

3. RESULTS AND DISCUSSION

3.1 Minority carrier electron lifetimes in p-GaAs on SiGe

Our prior work established a new standard for the structural and electronic quality of GaAs grown on Si with the establishment of minority carrier hole lifetimes for n-GaAs in excess of 10 ns.[1] While this is a good indicator of material quality expected for the base layer of a p/n configured cell, it is not indicative for the base region of an n/p cell. Hence, TRPL measurements were made on a series of p-type GaAs DH structures grown on GaAs and SiGe substrates with varying TDD values. Figure 1 shows the TRPL decays measured by monitoring the decay of the GaAs bandedge PL signal at 300K for samples doped to a nominal value of 2×10^{17} cm^{-3} to ensure relevance for the actual n/p cell structure. The impact of TDDs on the minority carrier electron lifetime is clearly demonstrated in this figure. Compared with the minority carrier hole lifetimes described elsewhere, the electron lifetimes are far more sensitive to TDD even for the highest quality SiGe substrates currently available; for the same TDD value (1×10^6 cm^{-2}) the electron lifetime is a factor of 5 lower than the hole lifetime, 1.8 ns and 10 ns respectively. However, as figure 2 shows, much like our earlier work on minority carrier hole lifetime, the electron lifetime follows the dependence expected for TDD limited lifetime. Hence, we conclude that residual dislocations from the substrate limit material quality and that other defects do not participate in limiting material quality for p-type GaAs on SiGe.

The fundamental reason for the lower electron lifetime and greater dependence on TDD becomes apparent upon consideration of the electron and hole minority carrier mobilities in GaAs, which result in diffusion coefficients of $D_n \sim 78$ cm^2/s for electrons and $D_p=7.1$ cm^2/s for holes.[6] In the context of the expression used to calculate the lifetime-TDD dependence,

$$\frac{1}{\tau} = \frac{1}{\tau_o} + \frac{\pi^3 D[TDD]}{4} \qquad (1)$$

a factor of 11 increase in D results in a substantial decrease in the net lifetime (in this expression, τ_o is the lifetime of the carrier in the absence of dislocations). Basically, the faster electrons, whose diffusion length is inherently longer than that

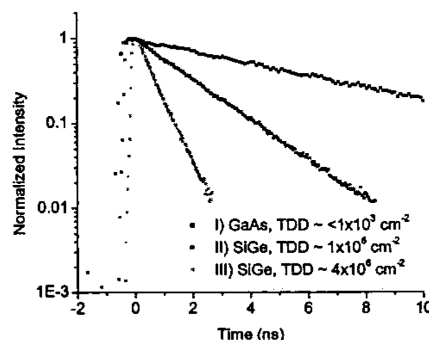

Figure 1: Time-resolved photo-luminescence decay curves for 0.5 μm p-type GaAs double heterostructures grown on various substrates.

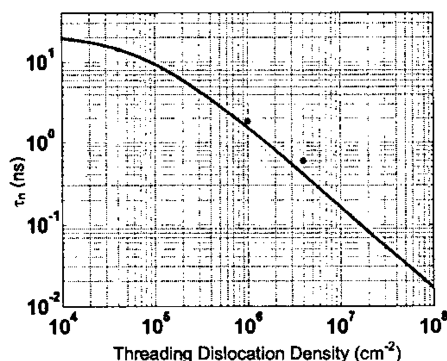

Figure 2: Theoretical curve for minority carrier electron lifetime in GaAs (2×10^{17} cm^{-3}) as a function of threading dislocation density. The two data points represent the experimentally determined values.

of holes due to their higher mobility, are able to more efficiently "sample" the background material and thus recombination of electrons at residual threading dislocations is enhanced. This results in an earlier dominance of the threading dislocation lifetime component for electrons compared to holes. If one considers the diffusion lengths for electrons and holes, L_{no} and L_{po} respectively, in GaAs in the absence of threading dislocations, and compares these values to the average threading dislocation spacing, L_{TD}, which can be calculated by assuming a uniform distribution of parallel threading dislocations dispersed within the GaAs bulk, one can appreciate the impact of TDD on minority carrier collection from n-type and p-type GaAs. For the homoepitaxial material at a doping of 2×10^{17} cm^{-3} the diffusion lengths for n-type and p-type GaAs are calculated to be $L_p \sim 4$ μm and $L_n \sim 20$ μm, in comparison, the value for L_{TD} at a TDD of 1×10^6 cm^{-2} is ~ 3.2 μm. As seen, the hole minority carrier diffusion length in GaAs without dislocations is already close to the L_{TD} value whereas the electron minority carrier diffusion length is much larger. However, at a TDD of 1×10^6

cm^{-2}, the net electron minority carrier diffusion length is found to be ~ 4 μm. While the dislocations clearly limits the electron diffusion length within the bulk p-type GaAs material, because the typical n/p cell base width is only ~ 2.5 – 3.5 μm, one can expect minimal impact on carrier collection, and hence on J_{sc}, over a limited range of residual TDD values. Indeed, results shown in the next section bear this out with the dominant effect of TDD variations observed to be on the cell V_{oc}.

3.2 n/p GaAs solar cells on SiGe substrates with low dislocation density

InGaP/GaAs single junction solar cells were grown and fabricated on two SiGe/Si substrates, one with a TDD value of $1x10^6$ cm^{-2} and another with a TDD value of $4x10^6$ cm^{-2} [7]. The n/p configuration as described earlier was used. Figure 3 shows AM0 J-V data obtained for these cells, which only differ in their residual TDD value. For the cell grown on the $1x10^6$ cm^{-2} TDD substrate, an AM0 efficiency of 13% and an AM1.5 efficiency of 15% were obtained. However, in comparing the two cells shown, some important observations can be made concerning the impact of TDDs on cell characteristics. First, it is clear that J_{sc} is not a strong function of the TDD over this range, confirming the discussion in the previous section regarding the dislocation-limited carrier collection in the base with respect to the base thickness.

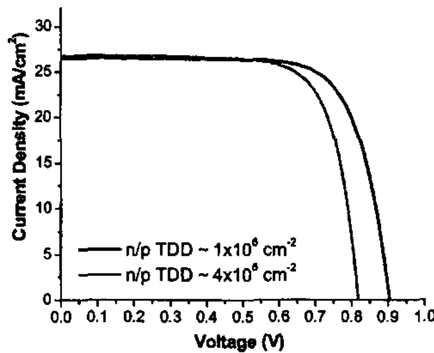

Figure 3: Light J-V response under AM0 conditions for representative single junction n/p cells grown on SiGe substrates with TDDs of $1x10^6$ cm^{-2} and $4x10^6$ cm^{-2}.

Quantum efficiency measurements (not shown), verify this, with no long wavelength degradation observed for the $4x10^6$ cm^{-2} TDD cells compared with the $1x10^6$ cm^{-2} TDD cells. In contrast, the impact on the V_{oc} value is very clear from figure 3. A factor of 4 reduction in TDD is observed to increase the V_{oc} by ~ 80 mV for identical cell structures. The strong dependence of V_{oc} on TDD can be understood by realizing that for GaAs solar cells and diodes, the saturation current is dominated by depletion region recombination for high quality diodes, and not by injection/diffusion processes. This is simply a consequence of the larger bandgap of GaAs, as compared to Si for example, so that the smaller value of n_i for GaAs reduces the injection/diffusion saturation current, which depends on n_i^2, far more strongly than it does the depletion region recombination component, which scales linearly with n_i. Simplifying the well-known expression for depletion region recombination current density, we can write,

$$J_o = 0.5qn_iW\frac{1}{\tau}. \qquad (2)$$

Here, W is the depletion region width and τ is the minority carrier lifetime. Since for the n/p cell, the doping is asymmetric such that the depletion region is ~ 90% within the p-side of the metallurgical junction, the lifetime term in equation 2 can be assumed to be the minority carrier electron lifetime within the p-type GaAs base. Inserting the values obtained for the lifetimes above at these TDD values translates into a factor of 3 decrease in the depletion region current density, consistent with the TDD reduction by a factor of ~4, given the uncertainty in such measurements. The reduced value for J_o for the lower TDD substrate ultimately is responsible for the increase in the cell V_{oc}, as observed.

Figure 4 shows a comparison of the light J-V data for a n/p solar cell grown on a SiGe/Si substrate with a TDD of $1x10^6$ cm^{-2} (as shown in figure 3) and one of our typical p/n cells grown on an n-type SiGe/Si substrate with the same TDD value. Again, a significant impact on V_{oc} is apparent. However, here, since the TDD values are identical, the higher V_{oc} for the p/n cell is attributed to the much higher minority carrier hole lifetime within the n-type base (10 ns), as opposed to the minority carrier electron lifetime in the p-type base (1.8 ns) of the n/p cell, resulting in a ~9-fold reduction in the depletion region recombination current density for the p/n cell. This in turn translates into a V_{oc} for the p/n cell (980 mV, AM0) that is ~10% higher than that for the n/p cell at the same TDD value. This fundamental difference between n/p and p/n cell performance dependence on TDD is expected to have important ramifications for the optimization of any III-V cell that is grown in the presence of residual dislocations from a lattice mismatched substrate, such as so-called "metamorphic" solar cells and other minority carrier devices.

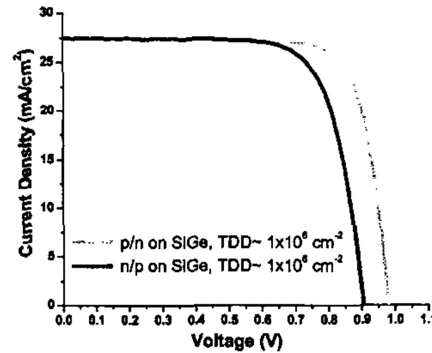

Figure 4: Light J-V response under AM0 conditions for representative single junction p/n and n/p cells grown on SiGe substrates with a TDD of $1x10^6$ cm^{-2}.

3.3 Large area p/n GaAs solar cells on SiGe substrates

In addition to development of n/p GaAs solar cells on SiGe/Si, another key issue has been the cell area. There has

been significant controversy concerning potential limitations on cell areas imposed by thermal expansion coefficient mismatches between the III-V epitaxial cell and Si substrates, since the tensile stress introduced by this mismatch during growth cooldown can generate wafer bowing stress-relieving microcracks within the III-V layers if those layers are beyond a critical thickness. Figure 5 shows a series of light J-V data obtained with an AM0 simulator for identically designed and grown single junction GaAs p/n cells as described above, as a function of cell area. As can be seen, the impact of increasing the cell area by more than a factor of 10 in this figure (a factor of 100 compared to our initial cells grown on SiGe/Si), is very small. Considering the V_{oc} and fill factor, the parameters expected to show the largest dependence on microcracks, values of 943 mV and 73.5% were obtained for the 0.36 cm^2 cell, compared with 942.4 mV and 73.1% for the 4 cm^2 cell. Moreover, the average deviation for the seven large area cells that were fabricated for this study was less than 2% for all cell parameters (note that this series of cells were grown on SiGe/Si substrates with TDD values of $\sim 2\times10^6$ cm^{-2}, which is a factor of 2 higher than the substrates which yielded 980 mV V_{oc} values for p/n cells; the slightly lower V_{oc} values for this series is due solely to this fact). This extremely close match for large and small cell areas, and the very small deviation in cell characteristics from device to device in spite of a low density (~ 200 μm average spacing) of fine microcracks within the cell, indicate that microcracks do not limit the solar cell parameters at this point of cell development. Hence, GaAs/SiGe cells with areas that are consistent with that necessary for various space and terrestrial applications based on GaAs/SiGe have been demonstrated.

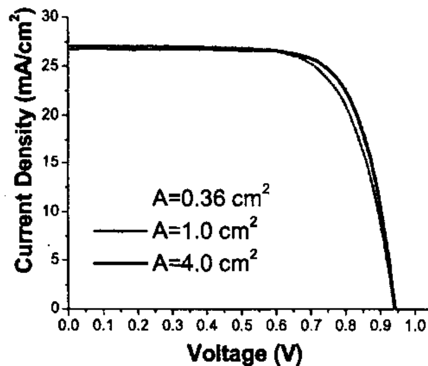

Figure 5: Light J-V response under AM0 conditions for representative single junction p/n cells for various device areas grown on SiGe substrates with a TDD of $\sim 2\times10^6$ cm^{-2}.

4. CONCLUSIONS

The first n/p configured GaAs cells have been grown, fabricated and tested on SiGe/Si substrates. Efficiencies in excess of 15% under AM1.5 conditions were obtained. A strong dependence of the cell V_{oc} on the substrate residual threading dislocation density was observed. Analysis attributed this strong dependence to the impact of the base electron minority carrier lifetime on the depletion region recombination current contribution to the reverse saturation current, which for p-type GaAs was measured to be much lower than the analogous hole lifetime in n-type GaAs. This fundamental difference between minority carrier electron and hole recombination is expected to have important ramifications on the choice of III-V solar cell polarity in the presence of dislocations. Finally, GaAs/SiGe cells spanning areas from 0.36 cm^2 to 4 cm^2 were fabricated, with negligible dependence on cell area being observed for cell performance.

5. ACKNOWLEGMENTS

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